PCT / IB 04 / 04394

PA 1257662

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

December 09, 2004

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: ***60/526,082***
FILING DATE: ***December 02, 2003***

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

P. R. Grant

P. R. GRANT
Certifying Officer

MODIFIED PTO/SB/16 (06-03)

U.S.PTO 60/526082 16018 12203

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

INVENTOR(S)			
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)	
Tan Hien BOON			Singapore
Wang Chuen KHIANG			Singapore
Rahamat BIDIN			Singapore
Anthony Sun YI SHENG			Singapore

☑ *Additional inventors are being named on the* 1 *separately numbered sheet(s) attached hereto*

TITLE OF THE INVENTION (500 characters max)

TRUE CHIP SCALE PACKAGE AND THE METHOD OF MAKING IT

CORRESPONDENCE ADDRESS

Direct all correspondence to the address for SUGHRUE MION, PLLC filed under the Customer Number listed below:

WASHINGTON OFFICE

23373

CUSTOMER NUMBER

ENCLOSED APPLICATION PARTS (*check all that apply*)

☑	Specification	*Number of Pages* 2	☐	CD(s), Number	
☑	Drawing(s)	*Number of Sheets* 4	☐	Other (specify)	
☐	Application Data Sheet. See 37 CFR 1.76				

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☑ A check or money order is enclosed to cover the Provisional filing fees. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to **Deposit Account No. 19-4880**. Please also credit any overpayments to said Deposit Account.

☐ The USPTO is hereby authorized to charge the Provisional filing fees to our **Deposit Account No. 19-4880.** The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to **Deposit Account No. 19-4880**. Please also credit any overpayments to said Deposit Account.

FILING FEE AMOUNT ($)
$160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE _____ DATE December 2, 2003

TYPED or PRINTED NAME Alan J. Kasper REGISTRATION NO. 25,426

TELEPHONE NO. (202) 293-7060 DOCKET NO. P78657

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

MODIFIED PTO/SB/16 (06-03)

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

Additional Page

Docket Number	P78657

INVENTOR(S)			
Given Name (first and middle if any])	Family Name or Surname	Residence (City and either State or Foreign Country)	
Rahul KAPOOR			Singapore
Desmond Chong Yok RUE			Singapore
Lim Leong CHEW			Singapore

*UTAC Invention Disclosure Number	
*Date of Disclosure	

*Official Use

UNITED TEST AND ASSEMBLY CENTER LTD
INVENTION DISCLOSURE FORM

1. Please submit all approved inventions to the Legal Department.
2. The Disclosure Form must be signed by all the inventors and the witnesses.
3. Please provide full details of the invention including the proper description and drawings. A soft copy of the Disclosure Form and the drawings should also be submitted together with the hard copy.

NAME OF INVENTION	True Chip Scale Package & The Method of Making It

	FULL NAME OF INVENTOR(S)	EMPLOYEE NUMBER	DEPARTMENT
1	Tan Hien Boon	80603	1530, Assy Devt
2	Wang Chuen Khiang	80027	1500, Assy Devt
3	Rahamat Bidin	80827	1530, Assy Devt
4	Anthony Sun Yi Sheng	80611	1500, Assy Devt
5	Rahul Kapoor	80044	1500, Assy Devt
6	Desmond Chong Yok Rue	80698	1500, Assy Devt
7	Lim Leong Chew	80346	1530, Assy Devt

Please provide the following information relating to the invention.

1. Background Information – How the invention or improvement is inspired, problems encountered or current practice that necessitated the invention or improvement.

Flip chip is one of the processing techniques for high performance/high I/O application. The flip chip enables single pass I/Os connection as compared with conventional wire bond interconnecting method. However, redistribution of I/Os is usually needed at wafer level, while such cost of redistribution is directly proportional to the total chip per wafer, while cost saving is also proportional to the number of I/Os. The invention explore the cheaper option of applying flip chip on products with such constraint, such as low I/Os memory product with relatively large die area (least number of chip per wafer), to enjoy the benefits of flip chip technique such as extreme low profile, high rate of data transfer, single pass/step interconnection etc.

2. Brief description of the invention or improvement.

The invention concept involves dicing of wafer into array of chips, such that multiple individual chips will form a larger chip panel. Such chips will have bumps present on the bond pads. The invention involve further processing of chip panel with flip chip concept onto a typical substrate/interposer of which re-distribution of I/Os is done, as well as potentially batch molding the multiple panels to enable presence of polymer based encapsulation/underfill to strengthen the structure for better reliability performance. Individual package is isolated in last step by conventional dicing method as in wafer processing.

3. Detail description of the invention or improvement. Please support with drawings whenever possible to illustrate the invention or improvement.

See attachment "PA1103-UTAC-P6 for illustration.

4. Other relevant information relating to the invention, if any.

N.A.

NAME OF INVENTOR(S)		SIGNATURE	DATE
1	Tan Hien Boon		
2	Wang Chuen Kiang		
3	Rahamat Bidin		
4	Anthony Sun Yi Sheng		
5	Rahul Kapoor		
6	Desmond Chong		
7	Lim Leong Chew		

APPROVED AND WITNESSED BY		SIGNATURE	DATE
1			
2			
3			

Patent Title : True Chip Scale Package & The Method of Making It

Detailed Description

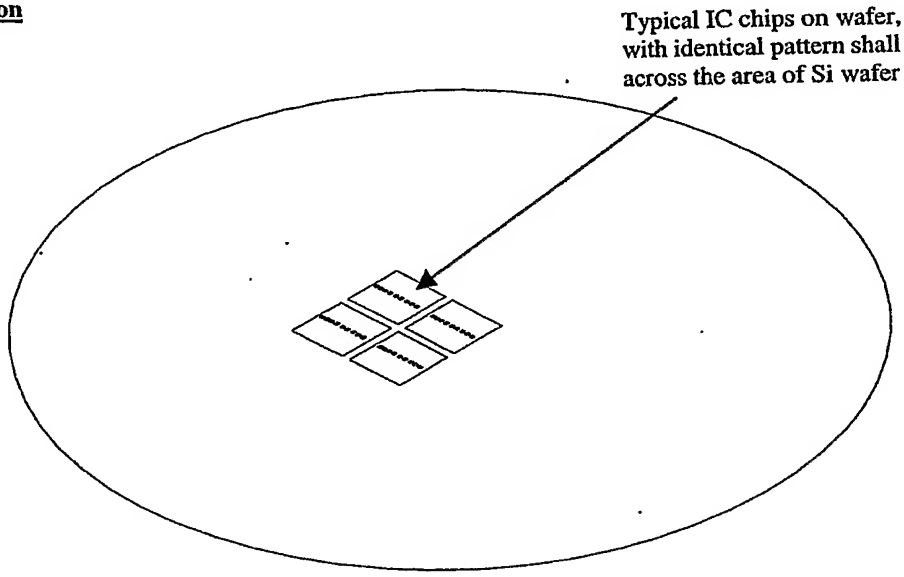

Figure 1

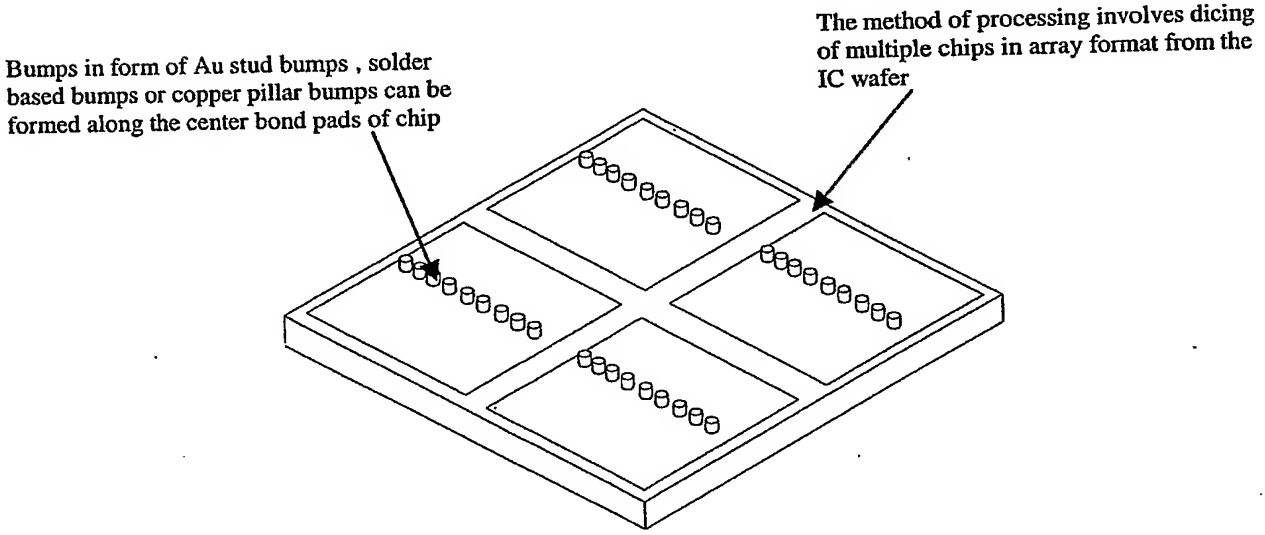

Figure 2

The chip (in form of multiple IC chips in array format) shall be flip-chip bonded onto a substrate/ interposer/film etc.

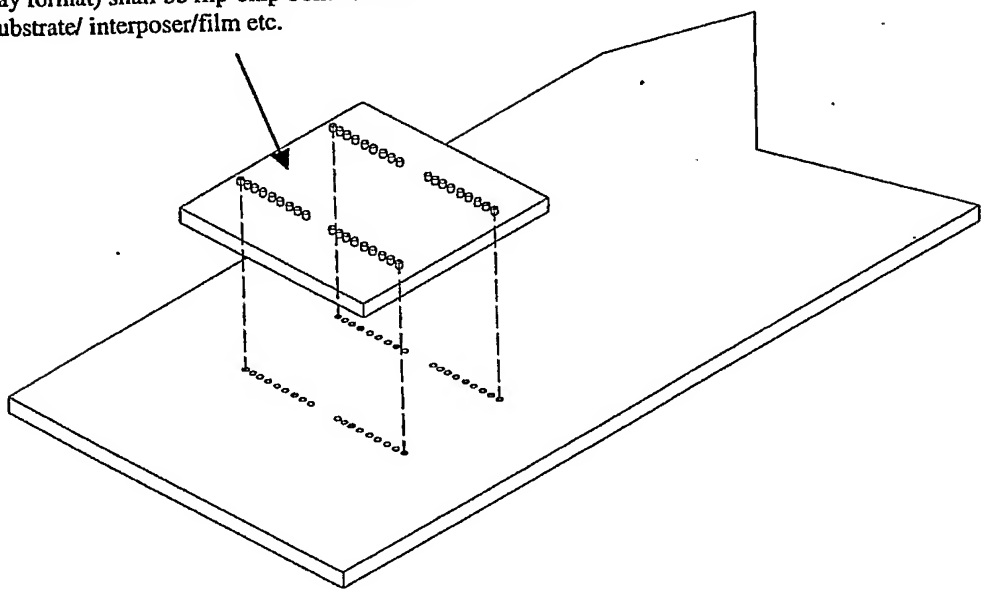

Figure 3

The substrate, acting as interposer shall re-distribute the I/Os into different format, e.g. in-line I/Os format can be redistributed into matrix array format

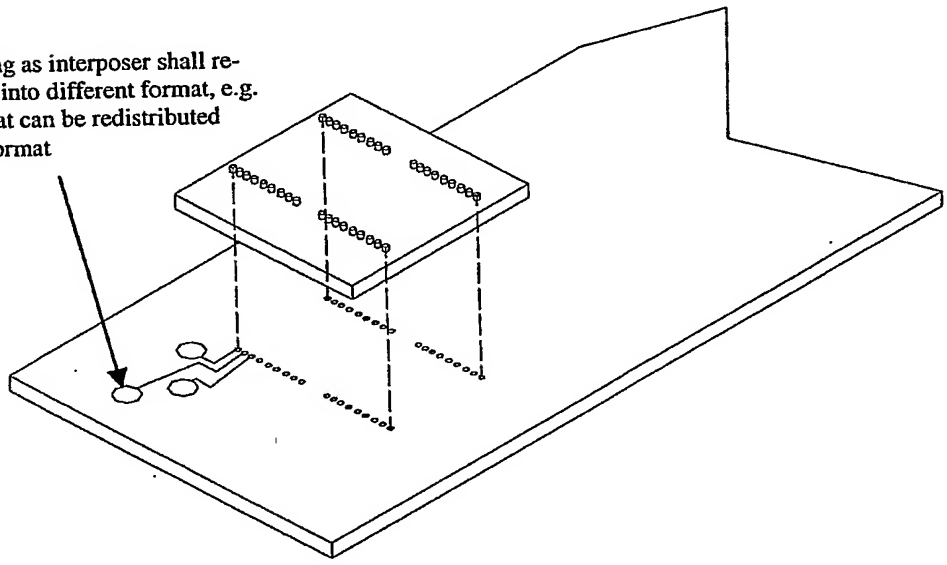

Figure 4

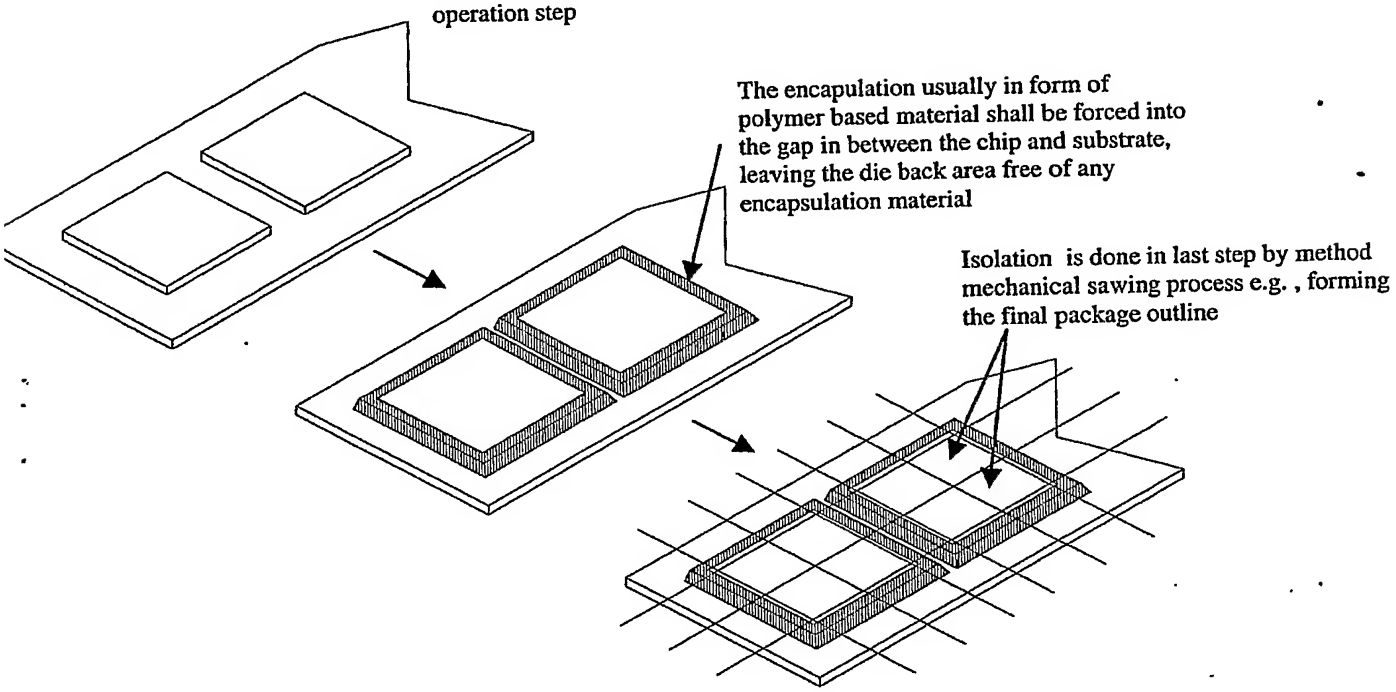

Figure 5

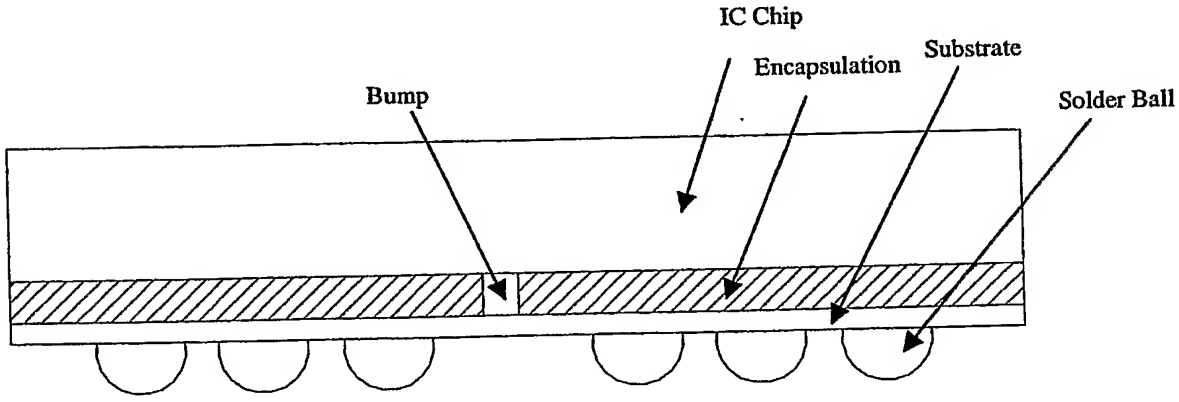

Figure 6

Figure 1 : Figure showing the typical wafers with repeated pattern of a typical IC chip. Wafer dicing is done to isolate certain "chip array" format, e.g 2x2, 3x3, 4x4 etc. Each chip may have e.g. in-line bond pads along the center of the chip, and solder/Au/copper pillar bumps may be present on bond pads for the necessary standoff required in subsequent processing.

Figure 2 : Figure 2 is showing a single "chip array" with presence of bumps on the bond pads/ Ios.

Figure 3 : Figure 3 shows the typical flip chip process, of which the chip array as illustrated in Figure 2 is connected to a typical substrate by flipping the chip to enable the interconnection.

Figure 4 : Figure 4 is showing the re-routing of the I/Os from in-line bond pads into form of matrix array, of which solder balls can be placed below the substrate to form subsequent connection to a typical printed circuit board. The substrate is serving as an interposer for such purpose.

Figure 5 : Figure 5 is showing the typical process of which a substrate with multiple panel of "chip array" shall be encapsulated such that the encapsulation (in form of compound or typical underfill material or polymer paste) will be present in between the active chip surface and susbtrate, as shown in Figure 6. The method of processing involves forcing of such underfill/compound material to flow in restricted channel only, without flowing to the back side of the chips. In last operation, the chip shall be isolated into individual package.

Figure 6 : Figure 6 shows the final package construction of which re-distribution of I/Os is done at substrate level under the total chip area.